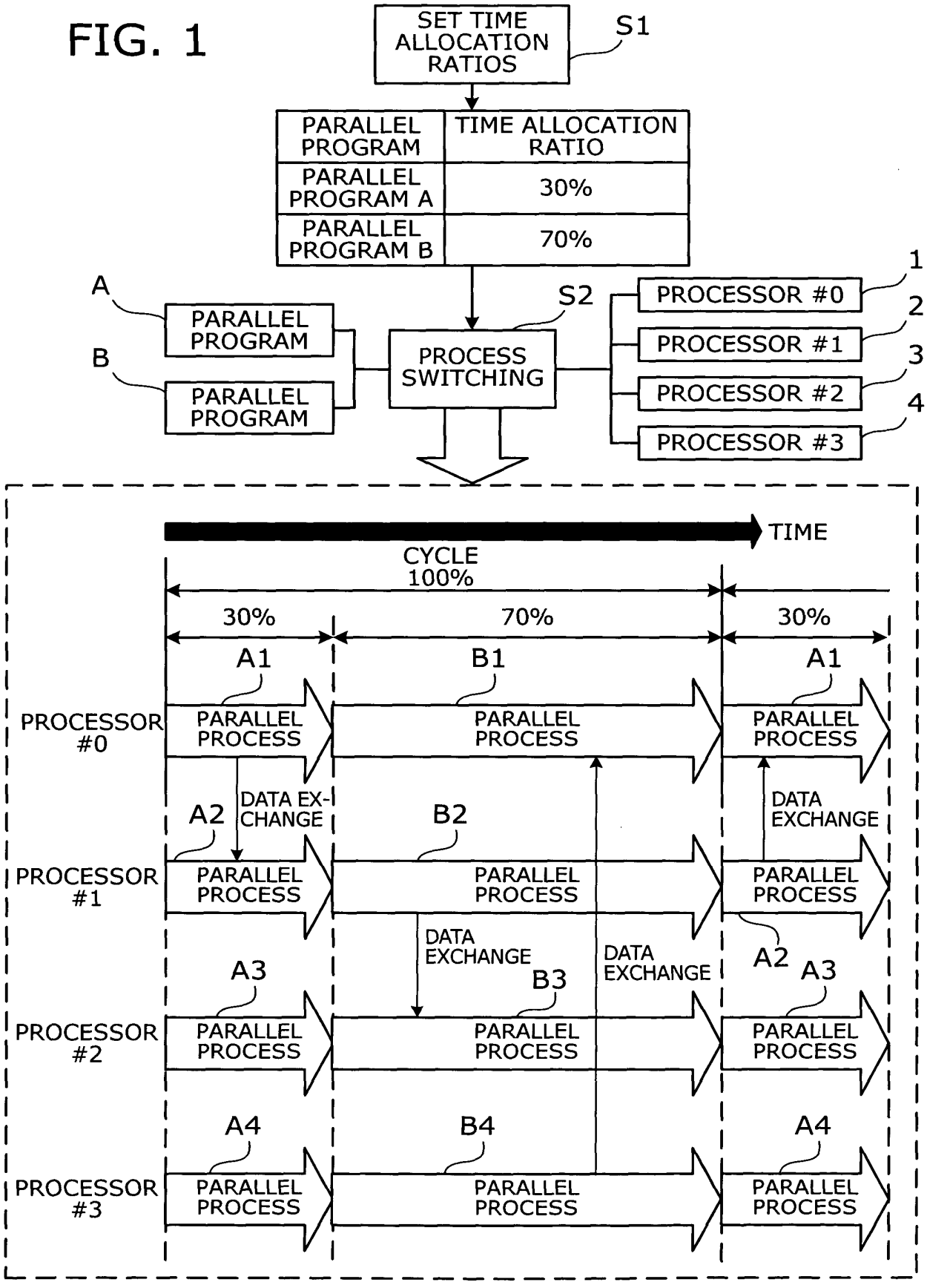
FIG. 1


SET TIME ALLOCATION RATIOS
S1
PARALLEL PROGRAM
TIME ALLOCATION RATIO
PARALLEL PROGRAM A
30%
PARALLEL PROGRAM B
70%
A
B
PARALLEL PROGRAM
PARALLEL PROGRAM
S2
PROCESS SWITCHING
PROCESSOR #0
PROCESSOR #1
PROCESSOR #2
PROCESSOR #3
1
2
3
4
TIME
CYCLE 100%
30%
70%
30%
A1
B1
A1
PROCESSOR #0
PARALLEL PROCESS
DATA EX-CHANGE
A2
B2
DATA EXCHANGE
PROCESSOR #1
DATA EXCHANGE
DATA EXCHANGE
A2
A3
B3
A3
PROCESSOR #2
A4
B4
A4
PROCESSOR #3

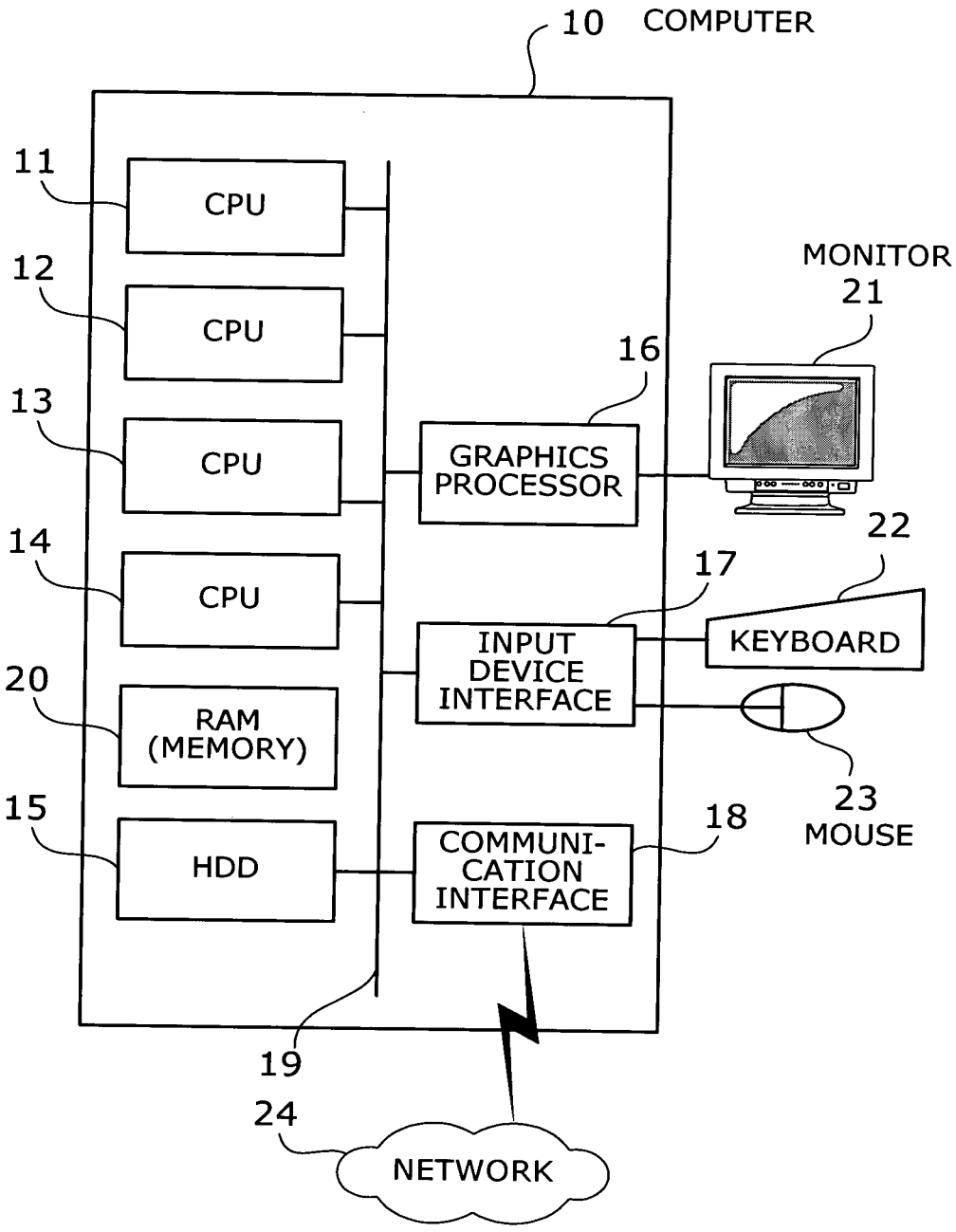

10 COMPUTER
11
CPU
12
CPU
13
CPU
14
CPU
20
RAM (MEMORY)
15
HDD
16
GRAPHICS PROCESSOR
17
INPUT DEVICE INTERFACE
18
COMMUNI-CATION INTERFACE
19
MONITOR
21
22
KEYBOARD
23
MOUSE
24
NETWORK

FIG. 2

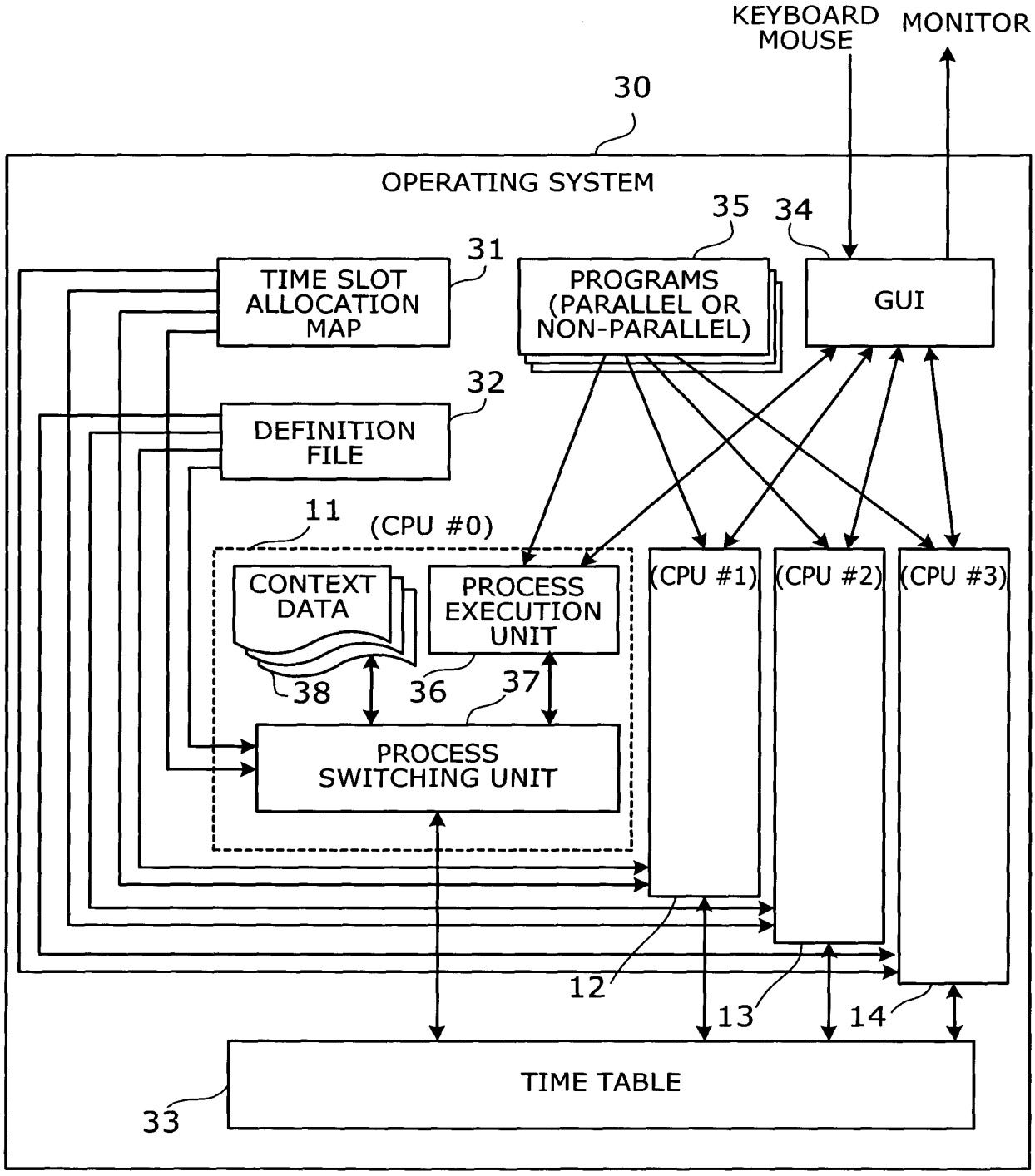

KEYBOARD
MOUSE
MONITOR
30
OPERATING SYSTEM
35
34
31
TIME SLOT ALLOCATION MAP
PROGRAMS (PARALLEL OR NON-PARALLEL)
GUI
32
DEFINITION FILE
11
(CPU #0)
CONTEXT DATA
PROCESS EXECUTION UNIT
(CPU #1)
(CPU #2)
(CPU #3)
38
36
37
PROCESS SWITCHING UNIT
12
13
14
TIME TABLE
33

FIG. 3

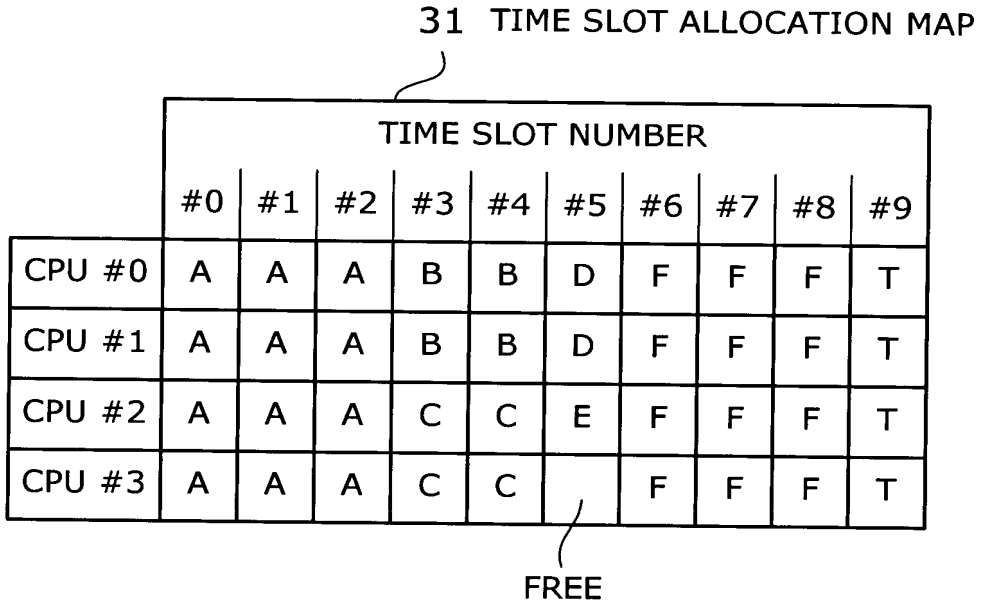
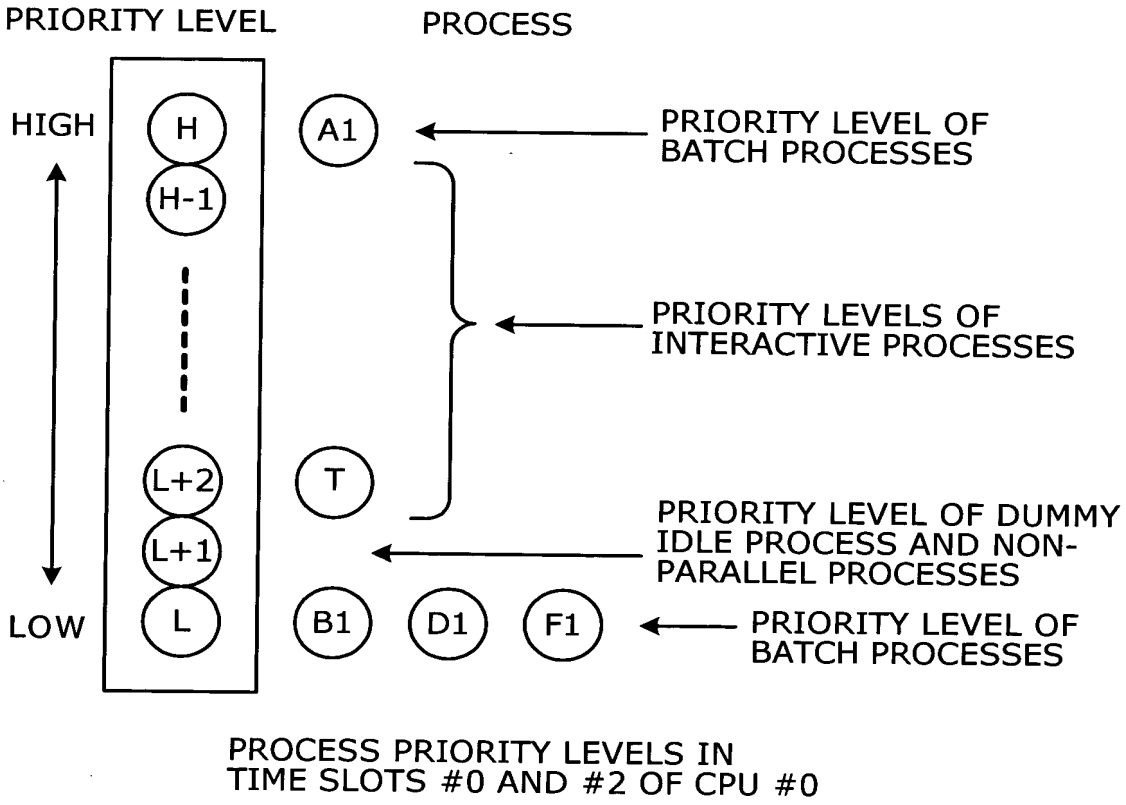

31 TIME SLOT ALLOCATION MAP
TIME SLOT NUMBER
#0 #1 #2 #3 #4 #5 #6 #7 #8 #9
CPU #0 A A A B B D F F F T
CPU #1 A A A B B D F F F T
CPU #2 A A A C C E F F F T
CPU #3 A A A C C F F F T
FREE

FIG. 4

33 TIME TABLE

TIME SLOT NUMBER	0	1	2	3	4	5	6	7	8	9
TIME OFFSET	+0 ms	+100 ms	+200 ms	+300 ms	+400 ms	+500 ms	+600 ms	+700 ms	+800 ms	+900 ms

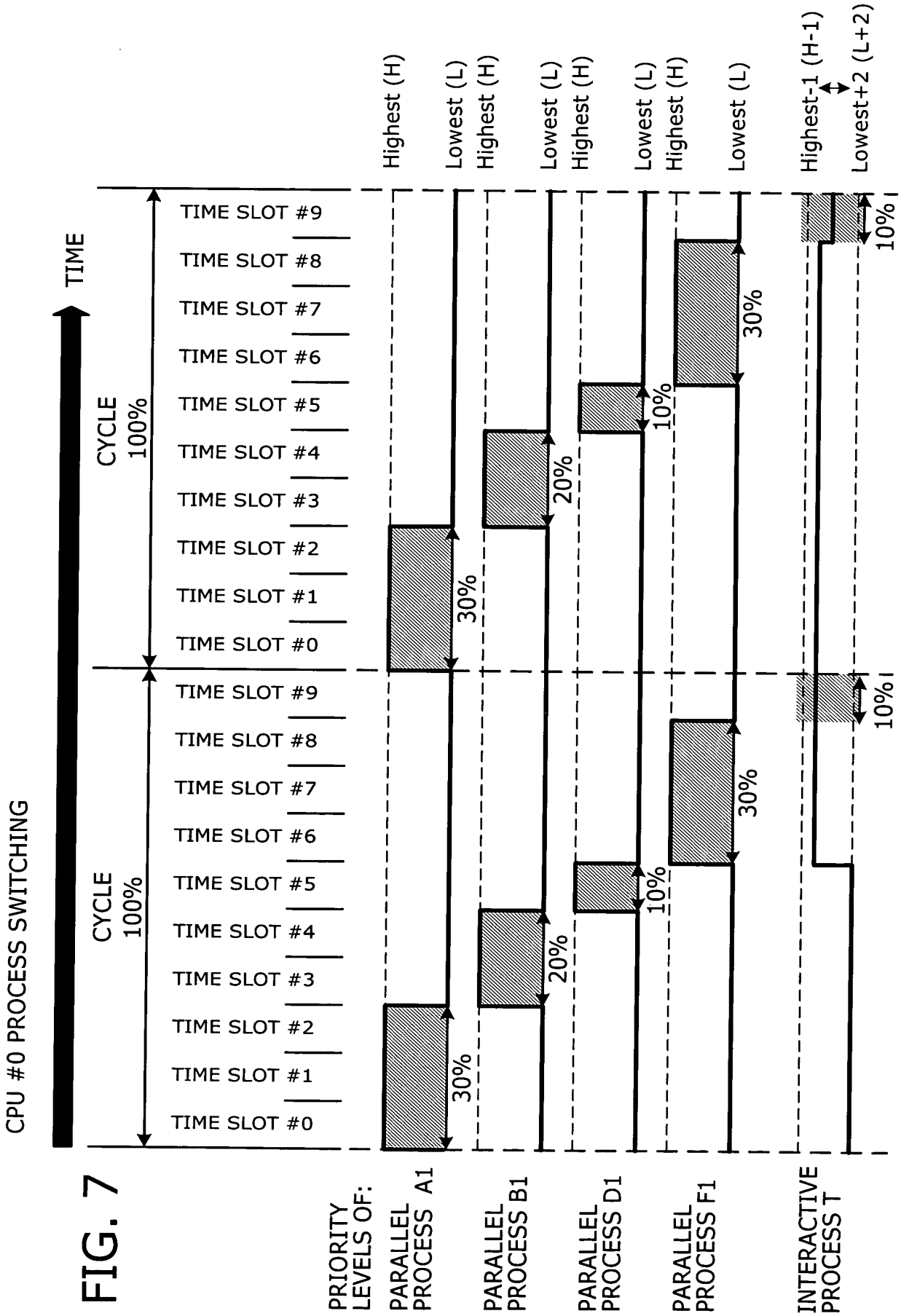
FIG. 5



PROCESS PRIORITY LEVELS IN TIME SLOTS #0 AND #2 OF CPU #0

FIG. 6

FIG. 7


CPU #0 PROCESS SWITCHING
TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
PRIORITY LEVELS OF:
PARALLEL PROCESS A1
PARALLEL PROCESS B1
PARALLEL PROCESS D1
PARALLEL PROCESS F1
INTERACTIVE PROCESS T
Highest (H)
Lowest (L)
Highest (H)
Lowest (L)
Highest (H)
Lowest (L)
Highest (H)
Lowest (L)
Highest-1 (H-1)
Lowest+2 (L+2)
30%
20%
10%
30%
20%
10%
30%
10%
30%
10%

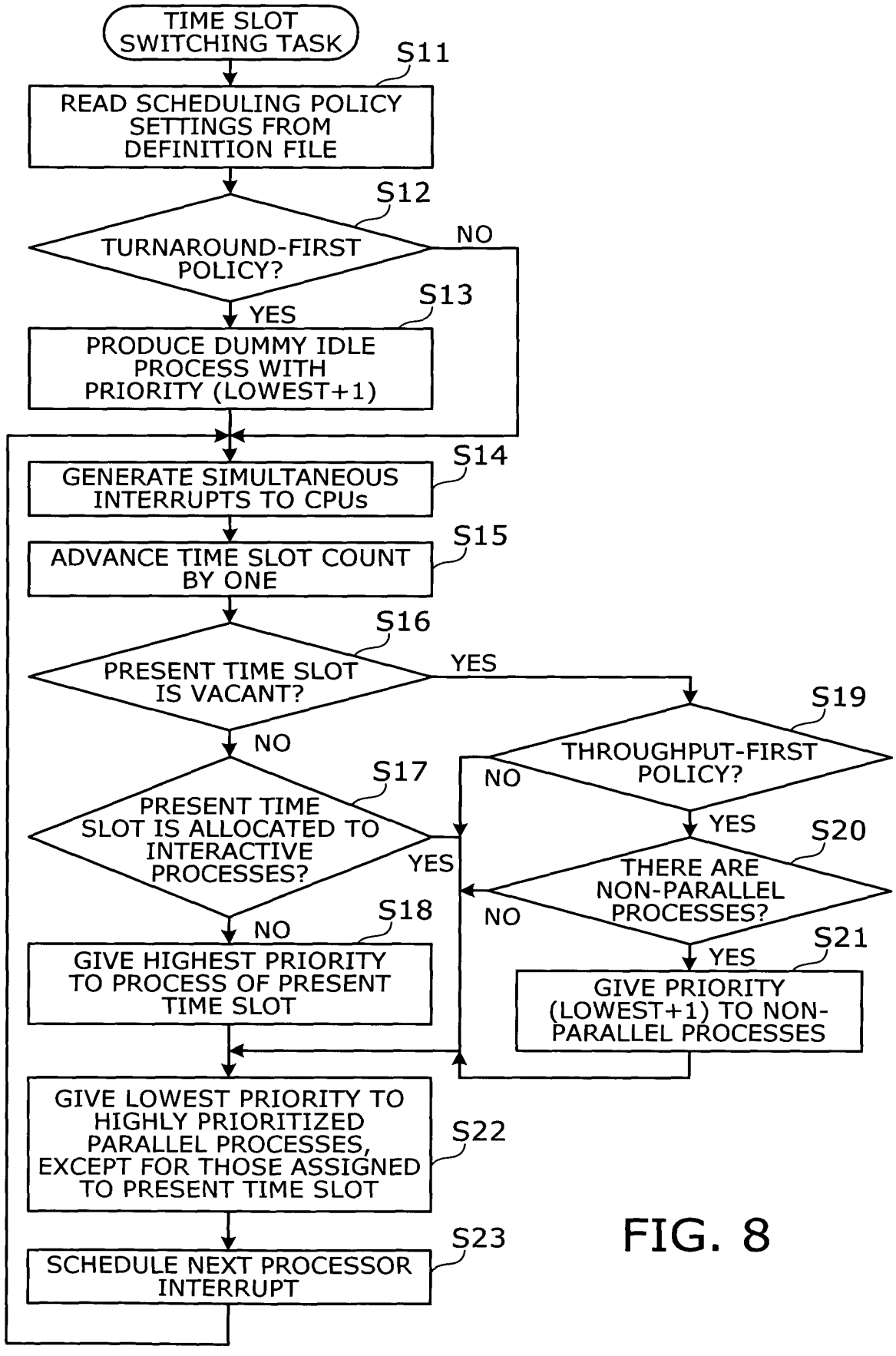

TIME SLOT SWITCHING TASK
S11
READ SCHEDULING POLICY SETTINGS FROM DEFINITION FILE
S12
TURNAROUND-FIRST POLICY?
NO
YES
S13
PRODUCE DUMMY IDLE PROCESS WITH PRIORITY (LOWEST+1)
S14
GENERATE SIMULTANEOUS INTERRUPTS TO CPUs
S15
ADVANCE TIME SLOT COUNT BY ONE
S16
PRESENT TIME SLOT IS VACANT?
YES
NO
S17
PRESENT TIME SLOT IS ALLOCATED TO INTERACTIVE PROCESSES?
YES
NO
S18
GIVE HIGHEST PRIORITY TO PROCESS OF PRESENT TIME SLOT
S19
THROUGHPUT-FIRST POLICY?
NO
YES
S20
THERE ARE NON-PARALLEL PROCESSES?
NO
YES
S21
GIVE PRIORITY (LOWEST+1) TO NON-PARALLEL PROCESSES
GIVE LOWEST PRIORITY TO HIGHLY PRIORITIZED PARALLEL PROCESSES, EXCEPT FOR THOSE ASSIGNED TO PRESENT TIME SLOT
S22
SCHEDULE NEXT PROCESSOR INTERRUPT
S23

FIG. 8

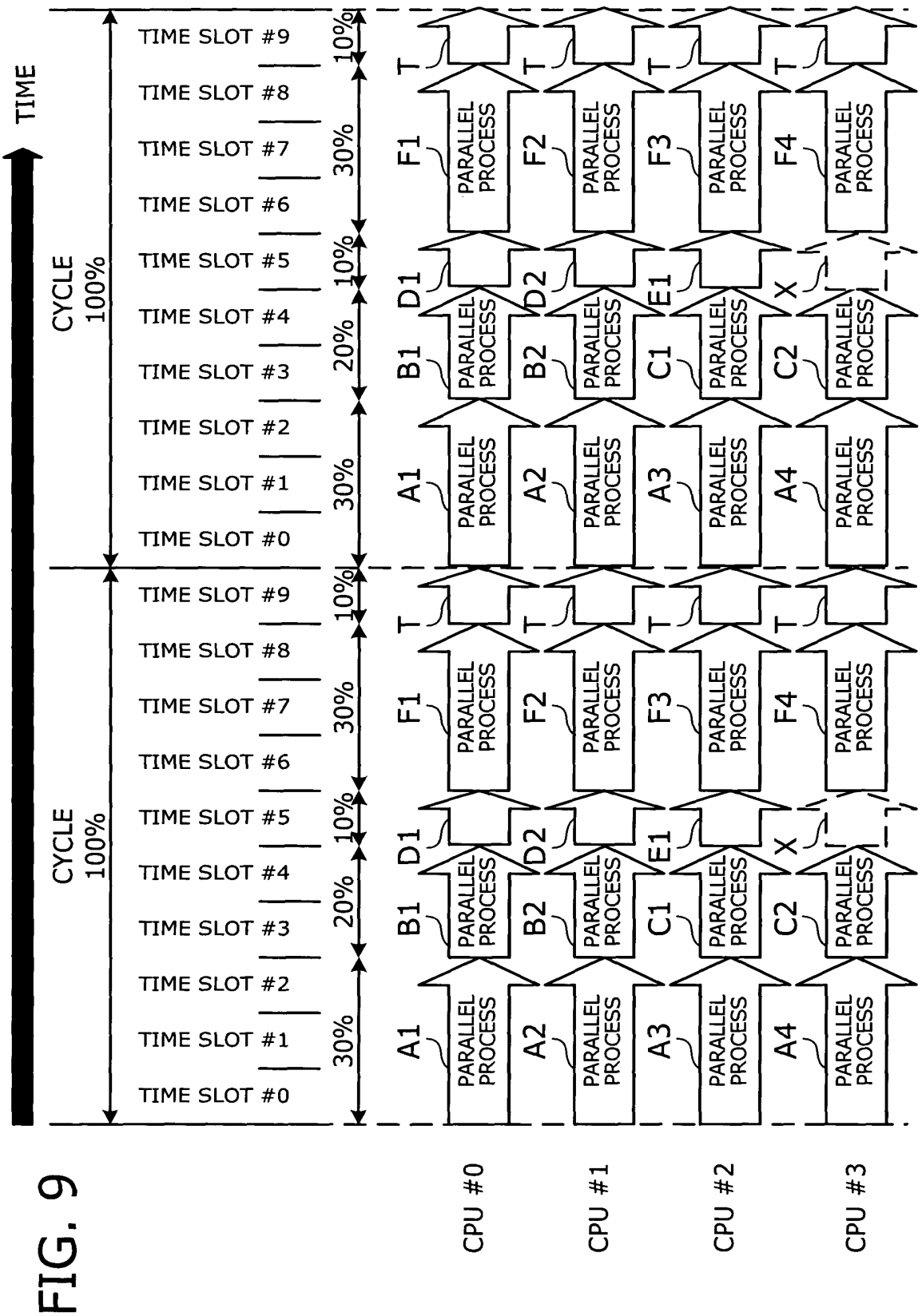

TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #0
TIME SLOT #1
TIME SLOT #2
TIME SLOT #3
TIME SLOT #4
TIME SLOT #5
TIME SLOT #6
TIME SLOT #7
TIME SLOT #8
TIME SLOT #9
30%
20%
10%
A1
B1
D1
F1
T
A2
B2
C1
D2
E1
F2
F3
X
A3
C2
A4
PARALLEL PROCESS
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 9

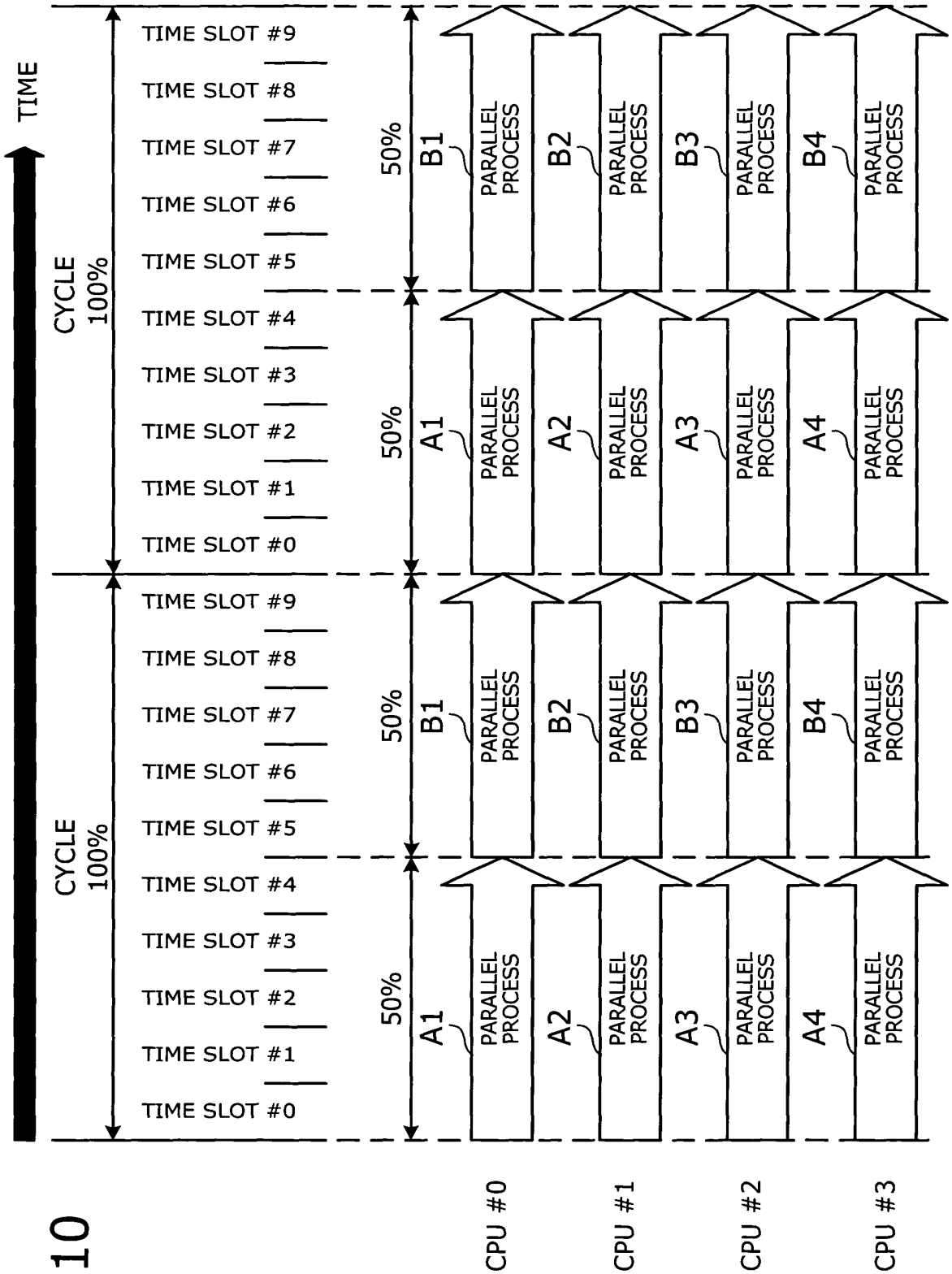

TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
50%
50%
50%
50%
B1
B2
B3
B4
A1
A2
A3
A4
PARALLEL PROCESS
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 10

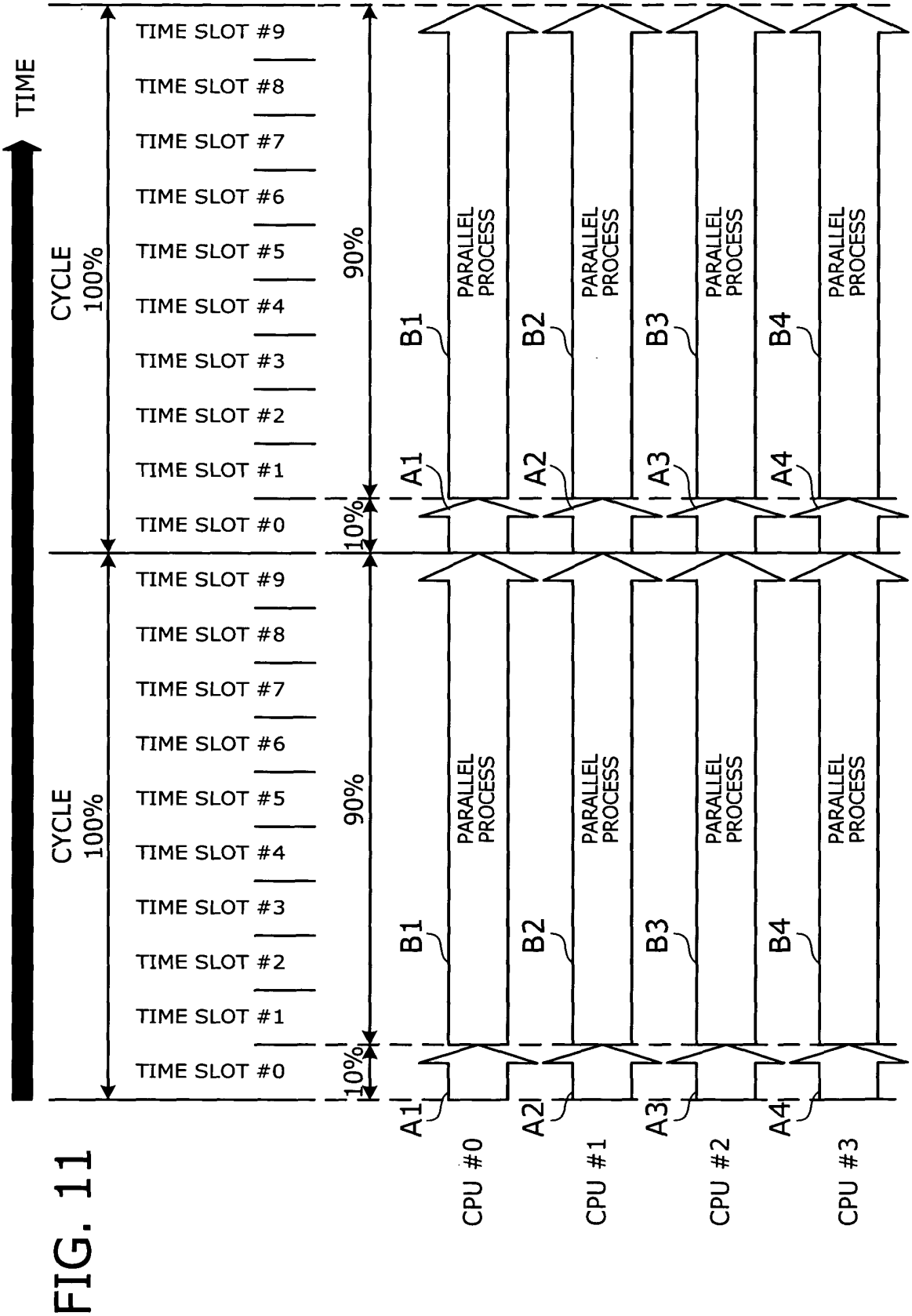

TIME
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
90%
10%
A1
A2
A3
A4
B1
B2
B3
B4
PARALLEL PROCESS
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 11

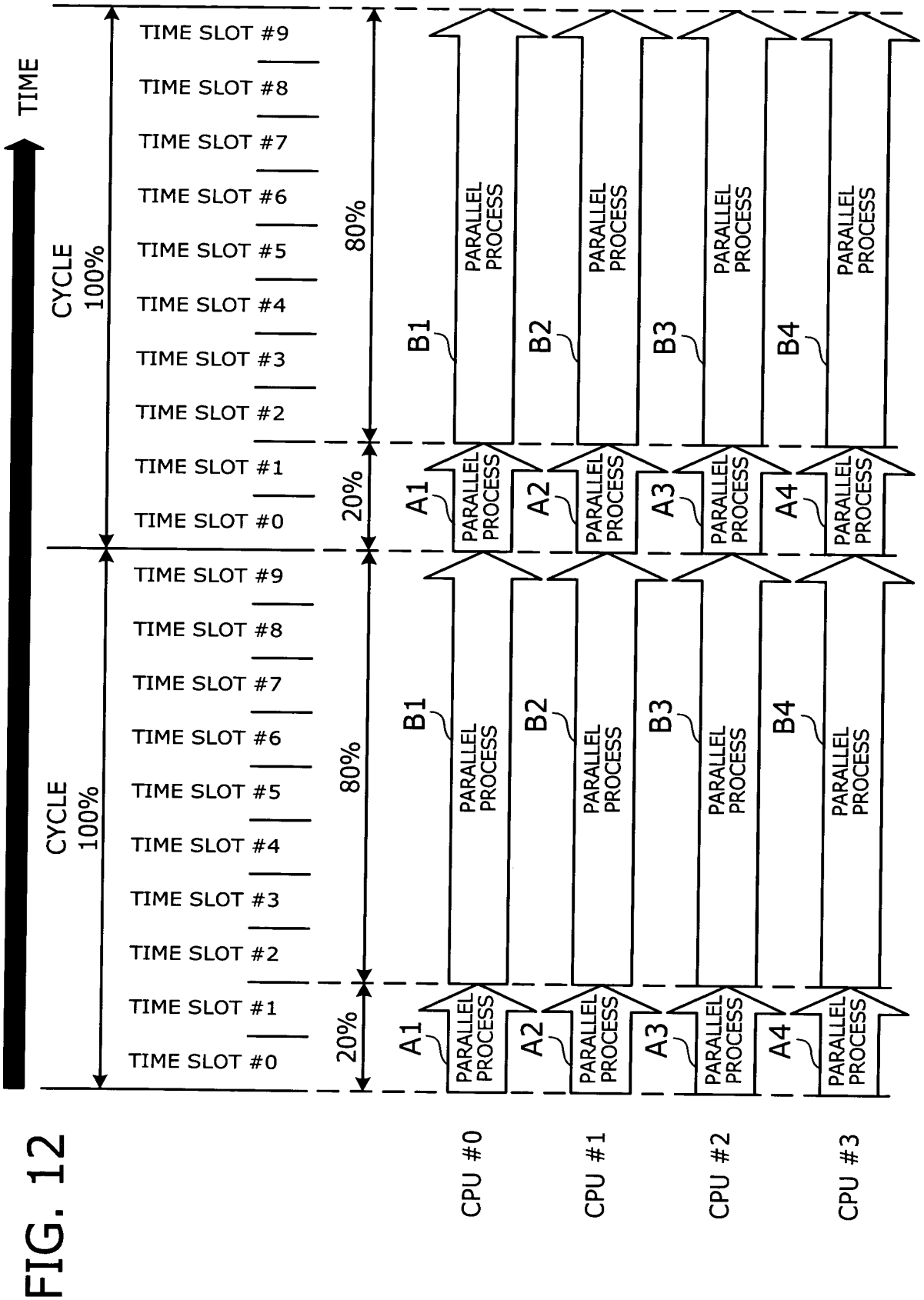

TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
80%
20%
80%
20%
B1
B2
B3
B4
A1
A2
A3
A4
PARALLEL PROCESS
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 12

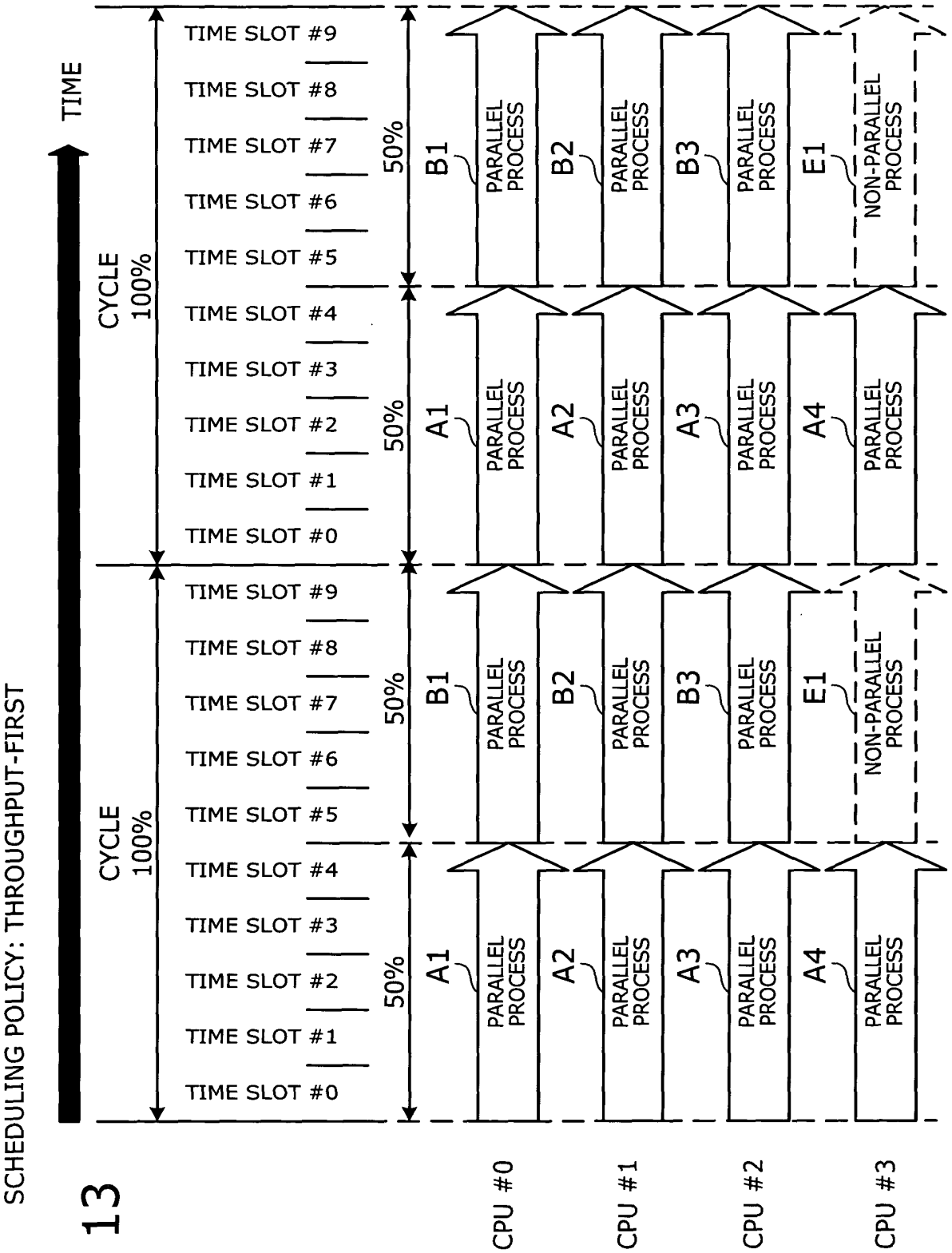

SCHEDULING POLICY: THROUGHPUT-FIRST
TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
50%
50%
50%
50%
A1
A2
A3
A4
B1
B2
B3
E1
PARALLEL PROCESS
NON-PARALLEL PROCESS
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 13

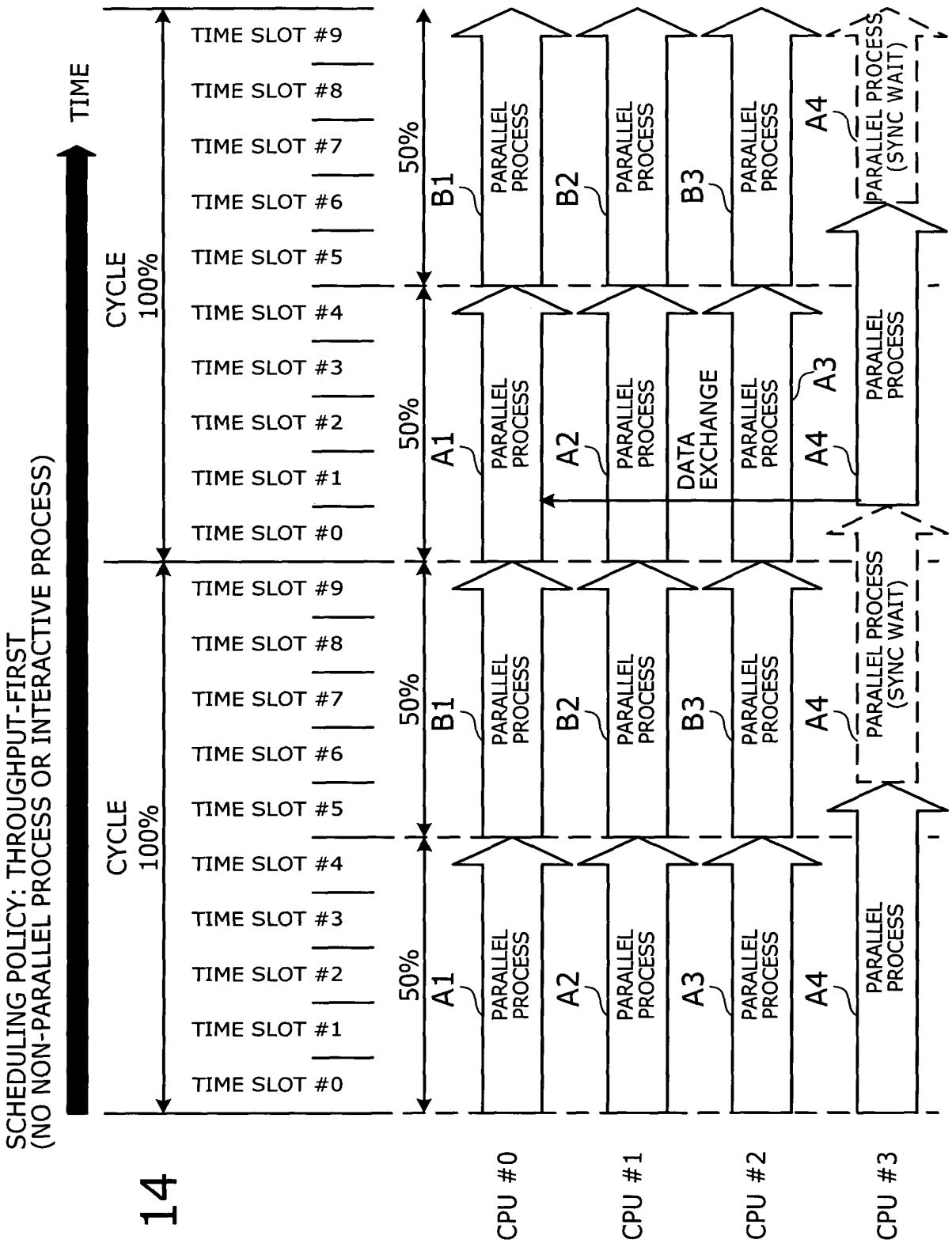

SCHEDULING POLICY: THROUGHPUT-FIRST
(NO NON-PARALLEL PROCESS OR INTERACTIVE PROCESS)
TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
50%
50%
50%
50%
A1
A2
A3
A4
B1
B2
B3
PARALLEL PROCESS
DATA EXCHANGE
PARALLEL PROCESS (SYNC WAIT)
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 14

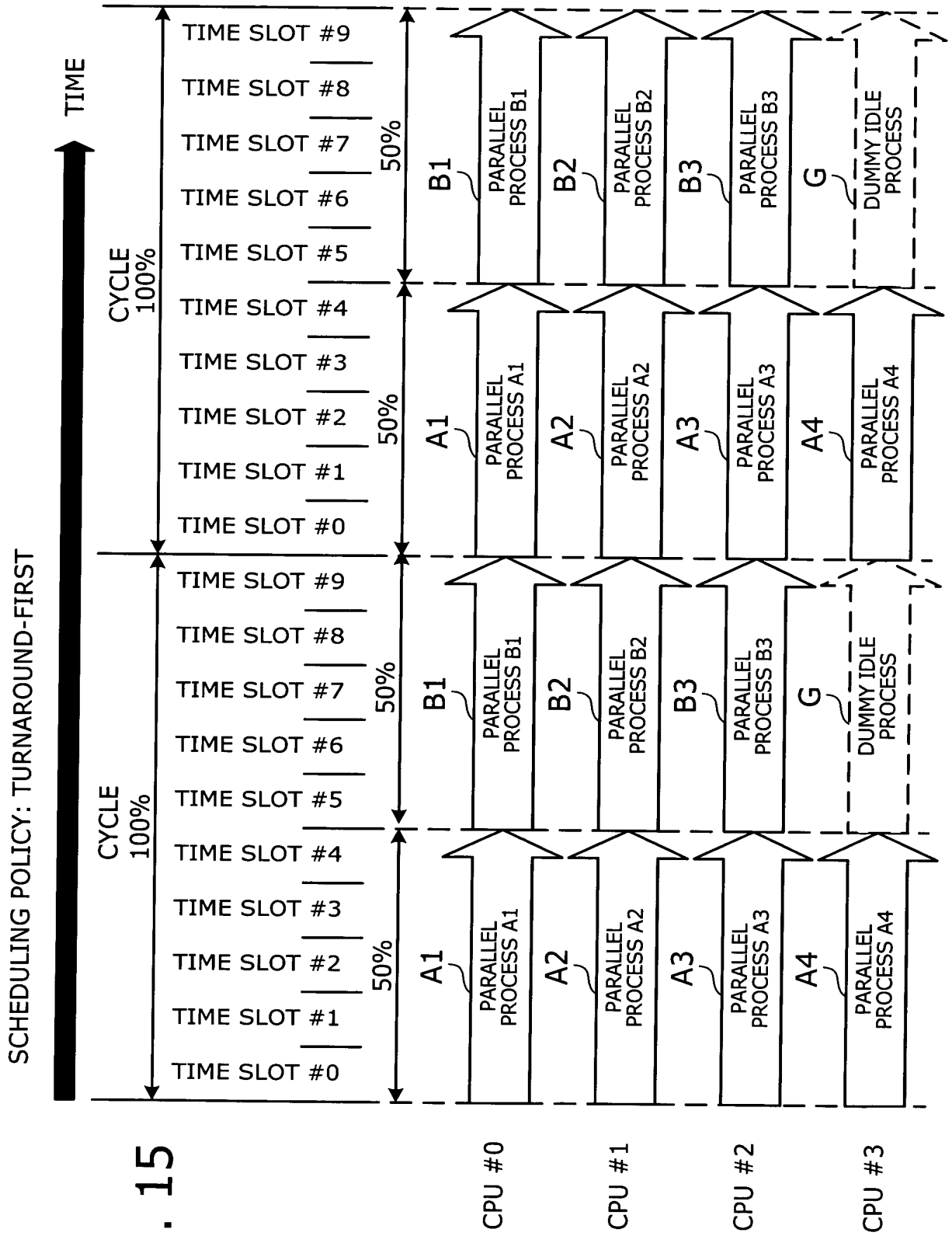

SCHEDULING POLICY: TURNAROUND-FIRST
TIME
CYCLE 100%
CYCLE 100%
TIME SLOT #9
TIME SLOT #8
TIME SLOT #7
TIME SLOT #6
TIME SLOT #5
TIME SLOT #4
TIME SLOT #3
TIME SLOT #2
TIME SLOT #1
TIME SLOT #0
50%
50%
50%
50%
B1
B2
B3
G
A1
A2
A3
A4
PARALLEL PROCESS B1
PARALLEL PROCESS B2
PARALLEL PROCESS B3
DUMMY IDLE PROCESS
PARALLEL PROCESS A1
PARALLEL PROCESS A2
PARALLEL PROCESS A3
PARALLEL PROCESS A4
CPU #0
CPU #1
CPU #2
CPU #3

FIG. 15

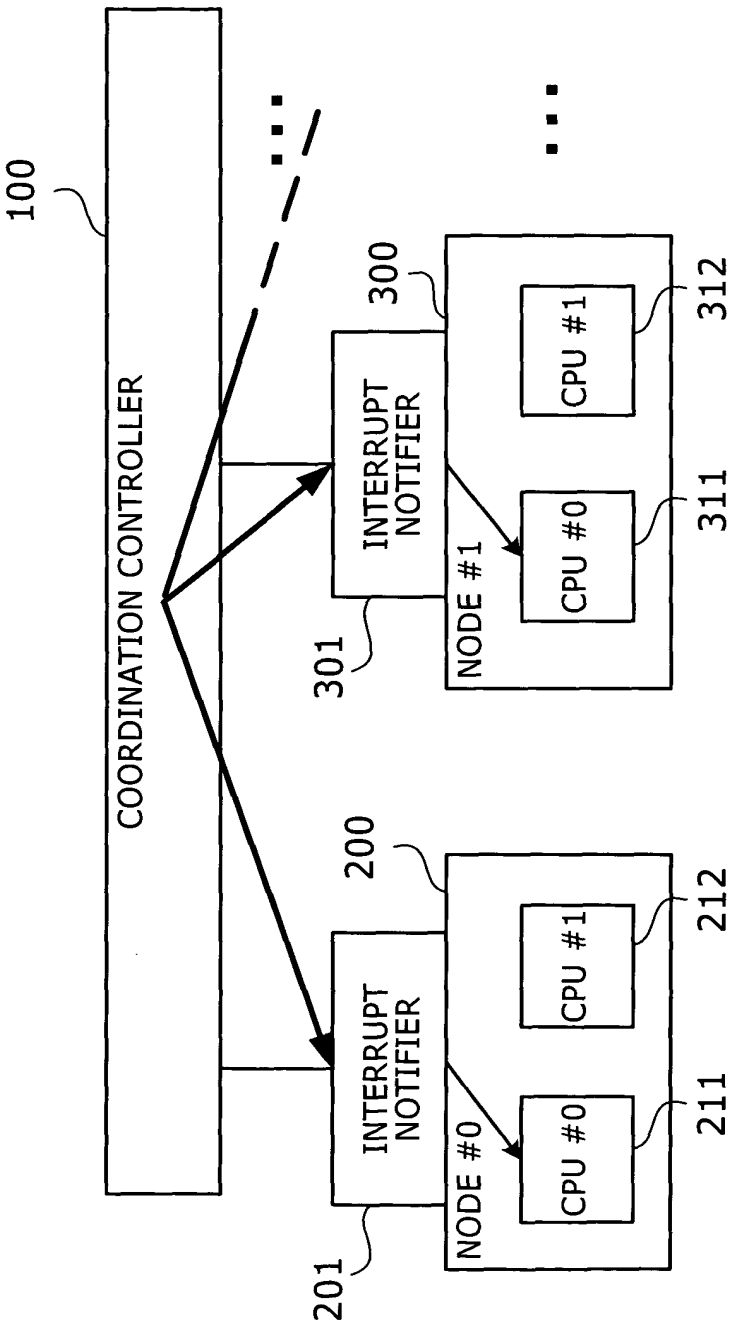

100
COORDINATION CONTROLLER
INTERRUPT NOTIFIER
INTERRUPT NOTIFIER
NODE #0
NODE #1
CPU #0
CPU #1
CPU #0
CPU #1
200
201
211
212
300
301
311
312

FIG. 16

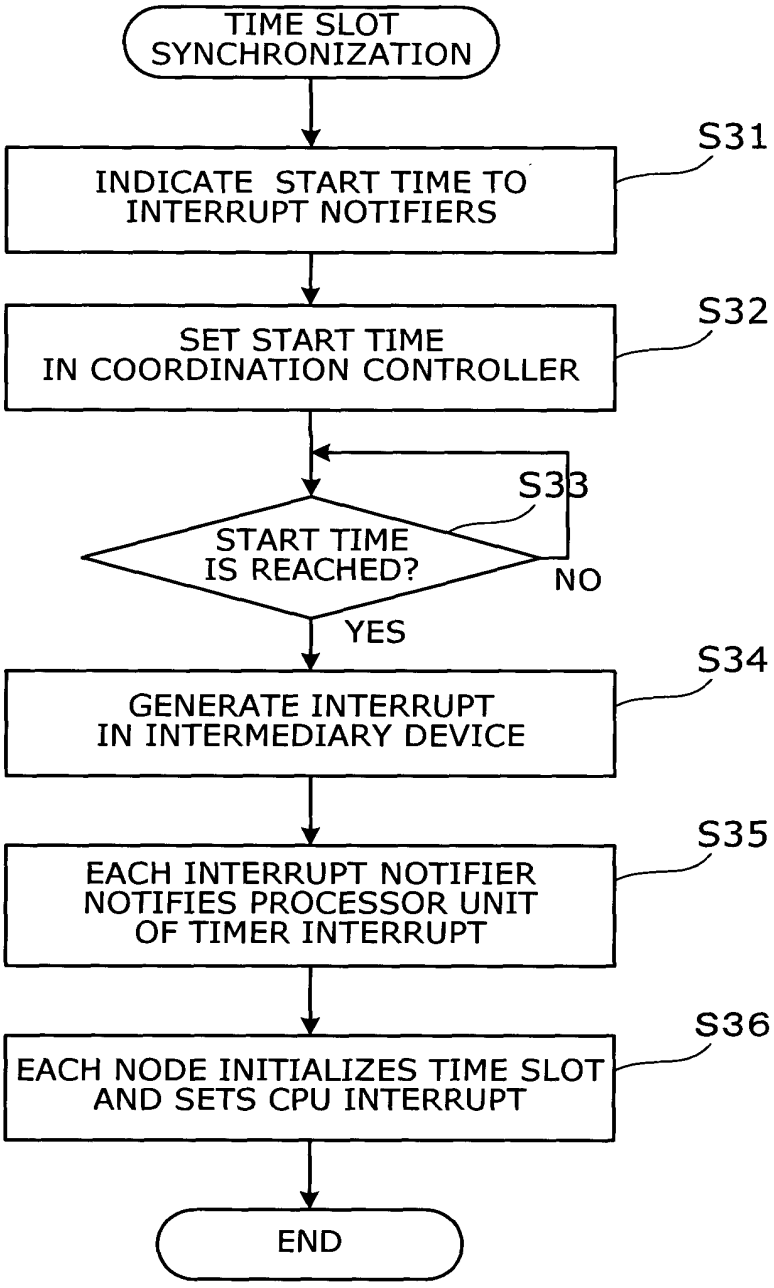
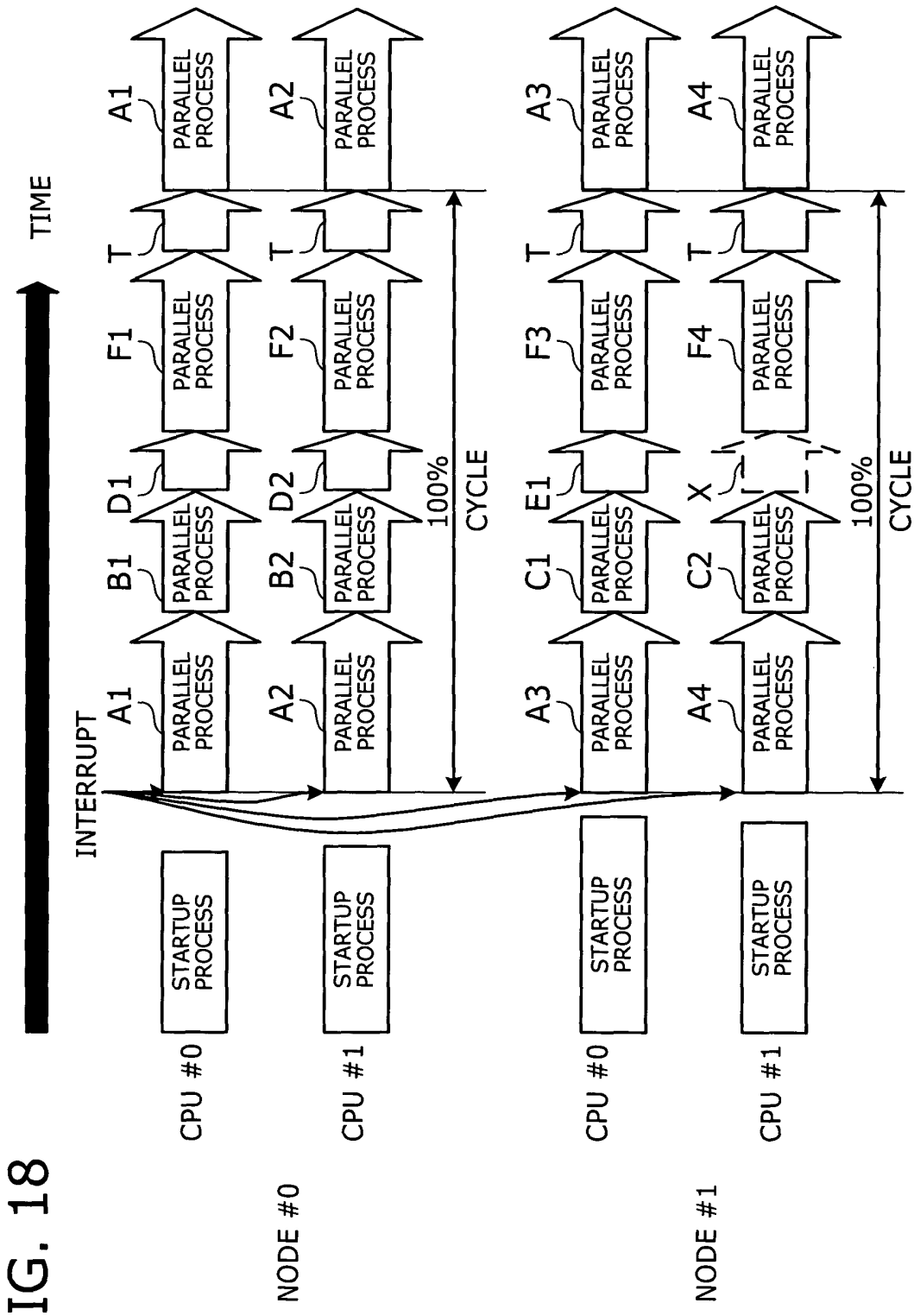

TIME SLOT SYNCHRONIZATION
INDICATE START TIME TO INTERRUPT NOTIFIERS
S31
SET START TIME IN COORDINATION CONTROLLER
S32
START TIME IS REACHED?
S33
NO
YES
GENERATE INTERRUPT IN INTERMEDIARY DEVICE
S34
EACH INTERRUPT NOTIFIER NOTIFIES PROCESSOR UNIT OF TIMER INTERRUPT
S35
EACH NODE INITIALIZES TIME SLOT AND SETS CPU INTERRUPT
S36
END

FIG. 17

FIG. 18


TIME
INTERRUPT
STARTUP PROCESS
CPU #0
CPU #1
NODE #0
NODE #1
A1
A2
A3
A4
B1
B2
C1
C2
D1
D2
E1
F1
F2
F3
F4
T
X
PARALLEL PROCESS
100% CYCLE